APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,542	01/05/2001	Randal N. Linden	1005/204	5270

				EXAMINER
530	7590	07/27/2004		RAMPURIA, SATISH

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		09/755,542	LINDEN, RANDAL N.
		Examiner	Art Unit
		Satish S. Rampuria	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is

closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>5-39</u> is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>5-39</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All   b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage

application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the amendment received on 04/30/2004 and has been

   entered.

2. Claims 1-4 have been canceled by the applicant. New set of claims 5-39 has been entered

   and are renumbered 1-34.

3. Claims 5-8, 10-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over US

   Patent No. 6,031,992 to Cmelik et al., hereinafter called Cmelik in view of US Patent No.

   6,708,325 to Cooke et al., hereinafter called Cooke.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cmelik and Cooke

   in view of Applicant's admitted prior art.

Specification

5. The objection of the title is still maintained and required corrective action. The title of the

   invention is not descriptive. A new title is required that is clearly indicative of the

   invention to which the claims are directed.

Claim Rejections - 35 USC § 112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

Claims 5, 24, and 32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply

with the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention. Regarding claims 5, 24, and 32, the limitation "automatically analyzing"

and "automatically generating" instructions are not supported by the specification.

The rejection of the base claim is necessarily incorporated into the dependent claims.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5, 24, 32, and 39 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

Clarification and/or correction are required.

Regarding, claims 5, 24, 32, and 39, the limitation, "determine a purpose" is unclear as to what

purpose needs to be achieved during the execution.

Regarding, claim 32, a ";" should be inserted at the end of each step signifying the end of a step

for clarity.

The rejection of the base claim is necessarily incorporated into the dependent claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5-8, 10-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No.

6,031,992 to Cmelik et al., hereinafter called Cmelik in view of US Patent No. 6,708,325 to

Cooke et al., hereinafter called Cooke.

Per claim 5:

Cmelik discloses:

-   A method of generating target instructions from a plurality of first instructions, the target

    instructions for execution on a target processor (col. 4, lines 41-44 "the target application

    is run on the host processor... a partial target operating system... which the target

    application generates"), comprising:

-   considered collectively, to determine a purpose to be achieved thereby (col. 2, 32-36 "the

    processor (interpreter) must be able to ensure that a primitive instruction (source) which

    requires data resulting from another primitive instruction is run after that other primitive

    instruction produces the needed (intended) data");

-   in preference over particular operations specified by individual ones of the plurality of

    first instructions (col. 9, lines 29-30 "to translate a set of target instructions into

    instructions of a host instruction set").

Cmelik does not explicitly disclose automatically analyzing the plurality of first instructions,

automatically generating the target instructions based on the automatically determined purpose.

However, Cooke discloses in an analogous computer system automatically analyzing the

plurality of first instructions (col. 2, lines 59-62 "a high level programming language compiler

automatically determines a set of one or more special instructions to extend the standard

instruction set of a microprocessor which will result in a relative performance improvement for a

given input computer program"), automatically generating the target instructions based on the

automatically determined purpose (col. 2, lines 33-36 "automatically compiles a computer

program written in a high level programming language into a program for execution by one or

more application specific integrated circuits coupled with a microprocessor").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate the method of automatically analyzing and automatically

generating the instructions as taught by Cooke into the method of generating instructions based

on the intended results as taught by Cmelik. The modification would be obvious because of one

of ordinary skill in the art would be motivated to automatically generate instructions for the

target processor to optimize the process of generating and executing code for the target processor

as suggested by Cooke (col. 1 and col. 2, lines 60-67 and lines 1-14).

Per claim 6:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the first instructions are not executable on the first processor (col. 3, lines 43-47

    "The emulator software changes the target instructions of an application program

written for the target processor family into host instructions capable of execution by the

host microprocessor").

Per claim 7:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

wherein the purpose is determined and the target instructions are generated at run-time, after

accessing the plurality of first instructions from a predetermined memory (col. 9, lines 23-26 "a

host computer designed to execute target programs for a target computer having a target

instruction set comprising the combination of software"), the method further comprising

executing the target instructions without requiring the target instructions to be first stored to the

predetermined memory (col. 12, lines 15-16 "host translates instructions into instructions for the

morph host on the fly").

Per claim 8:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein individual ones of the target instructions are generated without regard to

    particular operations specified by the individual ones of the plurality of first instructions

    (col. 9, lines 47-49 "to translate a new set of host instructions without the speculation

    when a set of host instructions fails to execute in accordance with the speculation").

Per claims 10 and 14:

The rejection of claims 5 and 12 are incorporated, respectively and further, Cmelik discloses:

- wherein the target instructions are generated in a manner to reduce a number of machine

    cycles required to execute the target instructions (col. 3, lines 51-57 "the host computers

    executing target programs using emulation software utilize reduced instruction set

    (RISC) microprocessors because RISC processors are theoretically simpler and

    consequently can run faster than other types of processors").

Per claims 11, 13, 15, and 23:

The rejection of claim 5 is incorporated, respectively, and further, Cmelik discloses:

- wherein the number of machine cycles is reduced in relation to the number of machine

    cycles that would be required to execute instructions according to a literal translation of

    the plurality of first instructions into the second machine language (col. 7, lines 63-65

    "the host operating system is already designed to respond to the same calls that the

    target application generates so that the generation of virtual devices is considerably

    reduced". Also, fig. 1(d) and related description.).

Per claims 12, 18, and 21:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the target instructions specify a target number of transfers between a register of

    the target processor and a memory associated with the target processor, the target

    number being reduced in relation to a number of transfers specified by the plurality of

    first instructions between a register of the first processor and memory associated with

    the first processor (col. 27, lines 52-65 "the length of the target instruction is added to

the value in the working instruction pointer register (Reip)... a commit instruction is

executed... the commit instruction copies the current value of each working register

which is shadowed into its associated official target register and moves a pointer value

designating the position of the gate of the gated store buffer from immediately in front

of the uncommitted stores to immediately behind those stores so that they will be placed

in memory").

Per claims 16 and 17:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein at least one of the target instructions is generated to specify a second physical

  operation that is different from, but equivalent to a first physical operation specified by

  one or more instructions of the plurality of first instructions (col. 8, lines 38-41 "maps

  the operations of the computer for which the application was designed to the hardware

  resources of the host machine in order to carry out the operations of the program being

  run").

Per claims 19, 20, and 22:

The rejection of claim 5 is incorporated, and further, Cmelik discloses:

- wherein the step of generating the target instructions includes eliminating operations

  specified by the plurality of first instructions which are unnecessary to achieve the

  determined purpose (col. 9, lines 34-39 "to optimize the instructions of the host

  instruction set translated from the target program speculating upon the occurrence of a

condition, means to determine under control of the software official state of the target

computer which existed at the beginning of a translation of a set of target instructions

during execution of the target program by the microprocessor").

Claims 24-31 are the computer program product claim corresponding to method claims 5, 7, 9,

12, 13, 15, 19, and 21 respectively, and rejected under the same rational set forth in connection

with the rejection of claims 5, 7, 9, 12, 13, 15, 19, and 21 respectively, above.

Claims 32-38 are the system claim corresponding to method claims 5, 9, 12, 13, 15, 19, and 21

respectively, and rejected under the same rational set forth in connection with the rejection of

claims 5, 9, 12, 13, 15, 19, and 21 respectively, above.

Claim 39 is the system claim corresponding to method claims 5, 6, 14, 15, and 16 respectively,

and rejected under the same rational set forth in connection with the rejection of claims 5, 6, 14,

15, and 16 respectively, above.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cmelik and Cooks

     in view of admitted prior art.

Per claim 9:

The rejection of claim 5 is incorporated, and further, neither Cmelik nor Cooks explicitly

disclose wherein the plurality of first instructions are according to a first machine language and

of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor.

However, admitted prior art discloses wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor (Applicant's specification, page 3, lines 3-9 "a target, will include an emulator that allows the target computer to emulate the instructions, called the source, of another type of CPU. Thus, the target computer will have stored in memory source instructions that may be called in response to applications software, target instructions emulating the source instructions and executable by the target CPU, and an emulator that causes one or more target instructions to be executed in response to a given source instruction. Thus, the given computer can execute target").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of having the independent instructions executing on host and target processor as taught in admitted prior art into the method of automatic analyzing and generating the instructions for the target processor as taught in combination system by Cmelik and Cooks. The modification would be obvious because of one of ordinary skill in the art would be motivated to have the independent instructions executing on the host and target processor to provide the less use of memory by the processors as suggested in admitted prior art (pages 5 and 6, lines 19-23 and 1-6, respectively).

Response to Arguments

9. Applicant's arguments with respect to claim 5 have been considered but they are not

persuasive.

In the remarks, the applicant has argued that:

For claim 5 cited reference does not suggest "automatically analyzing a plurality of first

instructions, considered collectively, to determine a purpose to be archived thereby and

automatically generating target instruction based on the automatically determined purpose, in

preference over particular operations specified by individual ones of the plurality of first

instructions", as claimed in claim 5.

Examiner's response:

It was noted by the applicant that the cited reference (Cmelik) disclose a method of dynamically

recompiling a set of instructions for execution on a target processor (see abstract). Therefore,

combination of new reference (Cmelik and Cooke) cited discloses the cited limitation,

automatically analyzing a plurality of first instructions, considered collectively, to determine a

purpose to be achieved thereby and automatically generating target instruction based on the

automatically determined purpose, in preference over particular operations specified by

individual ones of the plurality of first instructions, therefore, claims (see rejection of claims 5,

24, and 32 above) are rejected in this office action. Furthermore, since it appear the applicant's

relies on what is known in the art for support (see item 5 in this office action) it would have been

obvious to utilize the feature in Cmelik system to automatically analyzing a plurality of

instructions and automatically generating target instruction to dynamically recompiling a set of

instructions for execution on a target processor.

Conclusion

10. Applicant's amendment necessitated the rejection presented in this office action.

Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the

extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing
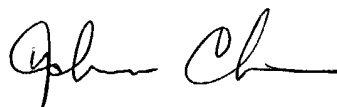
date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to **Satish S. Rampuria** whose telephone number is **703-305-8891.**

The examiner can normally be reached on **8:30 am to 5:00 pm.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, **Kakali Chaki** can be reached on **(703) 305-9662.** The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit 2124
07/12/2004

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124